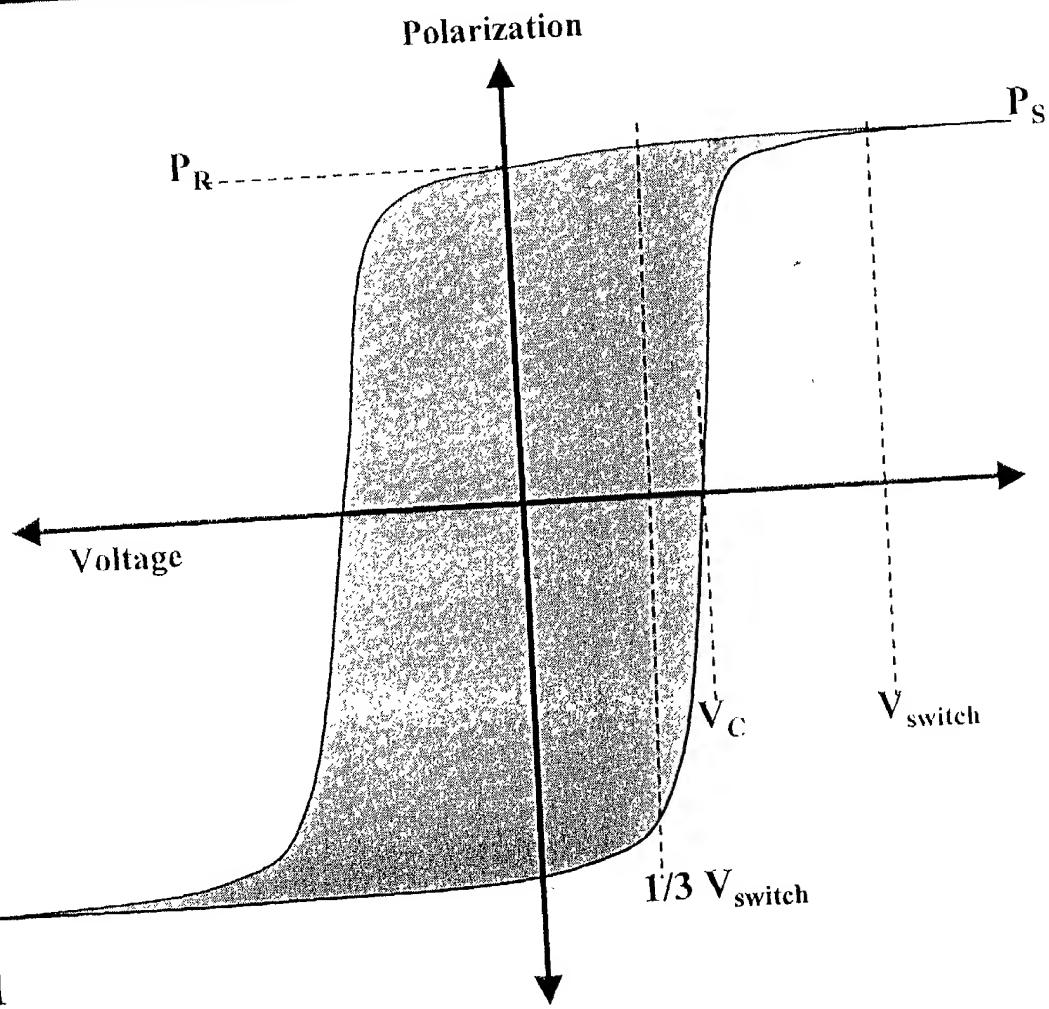


Fig.1

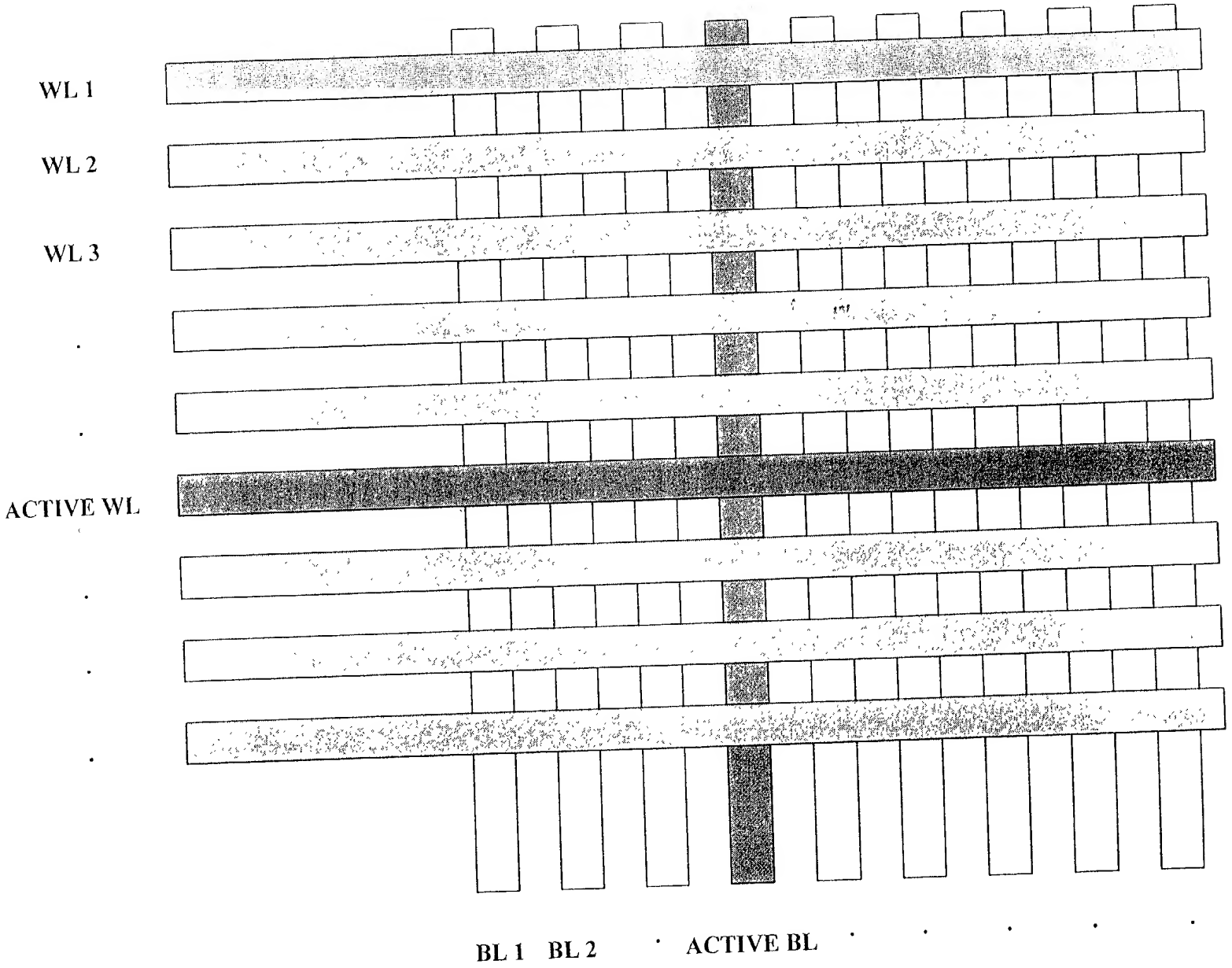


FIG.2

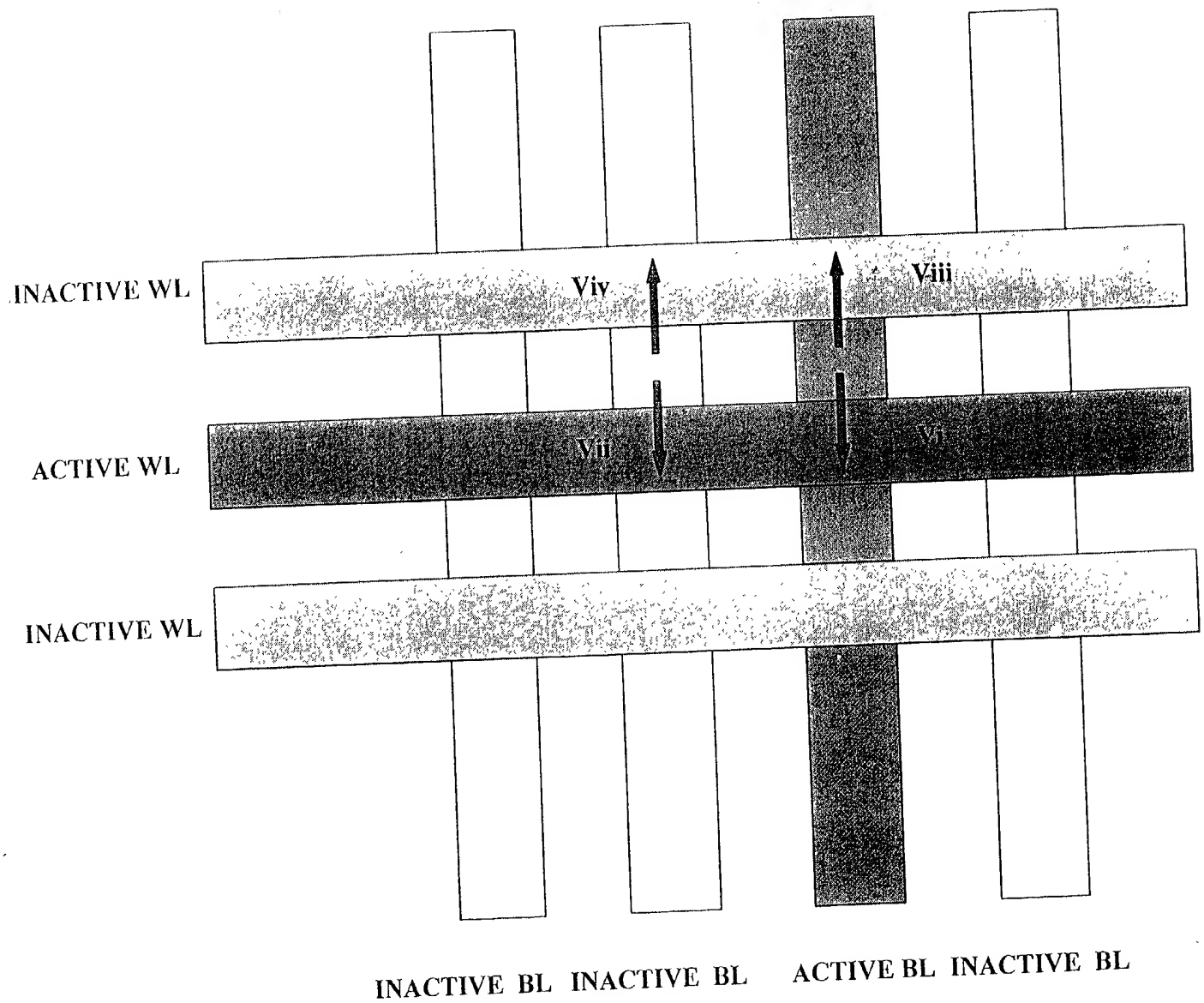
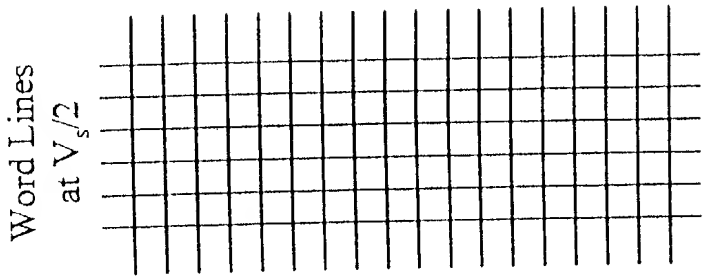


FIG.3

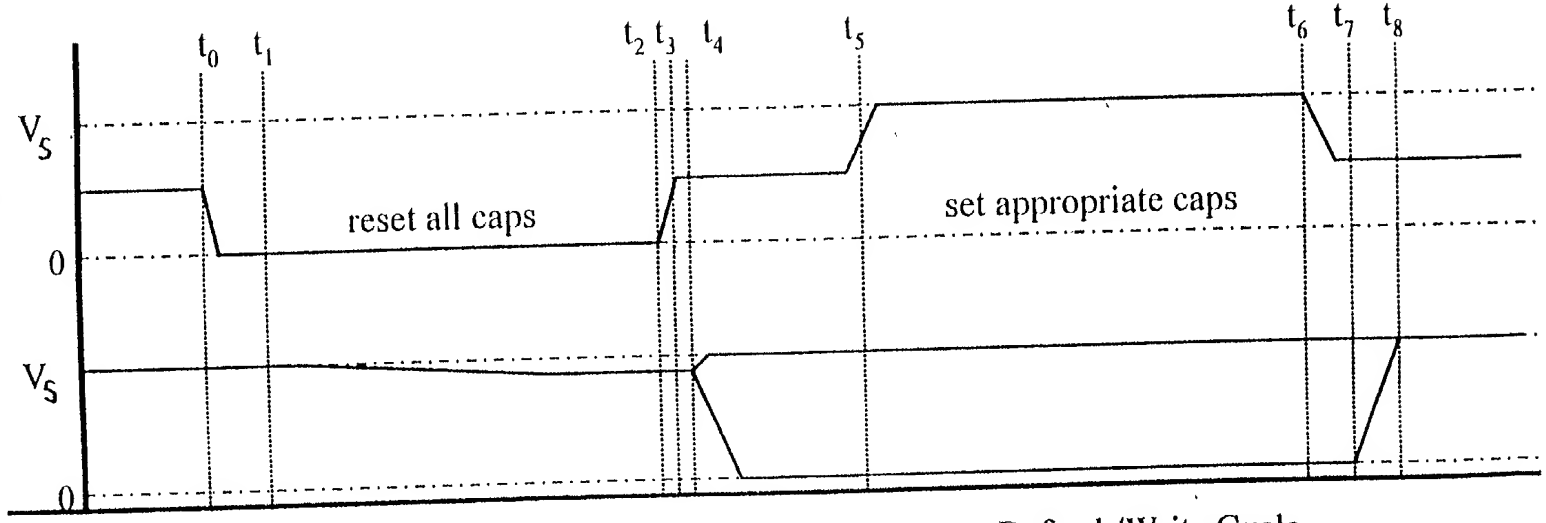
3 Level Passive Matrix Switching Protocol

- t_0: word line latched, active pulldown to 0
- t_1: bit line clamp released - sense amp on
- t_2: bit line decision - data latched
- t_3: word line returned to quiescent $V_s/2$
- t_4: write data latched on bit lines
- t_5: word line pulled to V_s - set/reset caps
- t_6: word line returned to quiescent $V_s/2$
- t_7: bit lines actively returned to V_s clamp
- t_8: read/write cycle complete

Maximum depolarizing voltage Vs/2



Sense Amps biased near V_s



Read Cycle

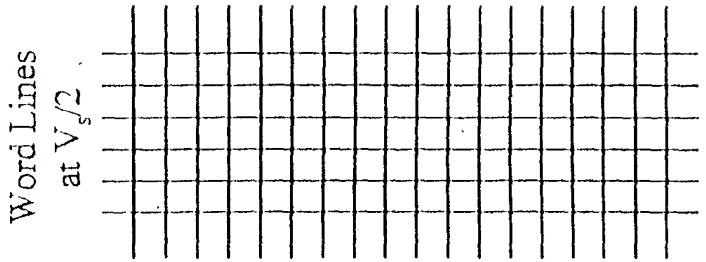
Refresh/Write Cycle

FIG. 4

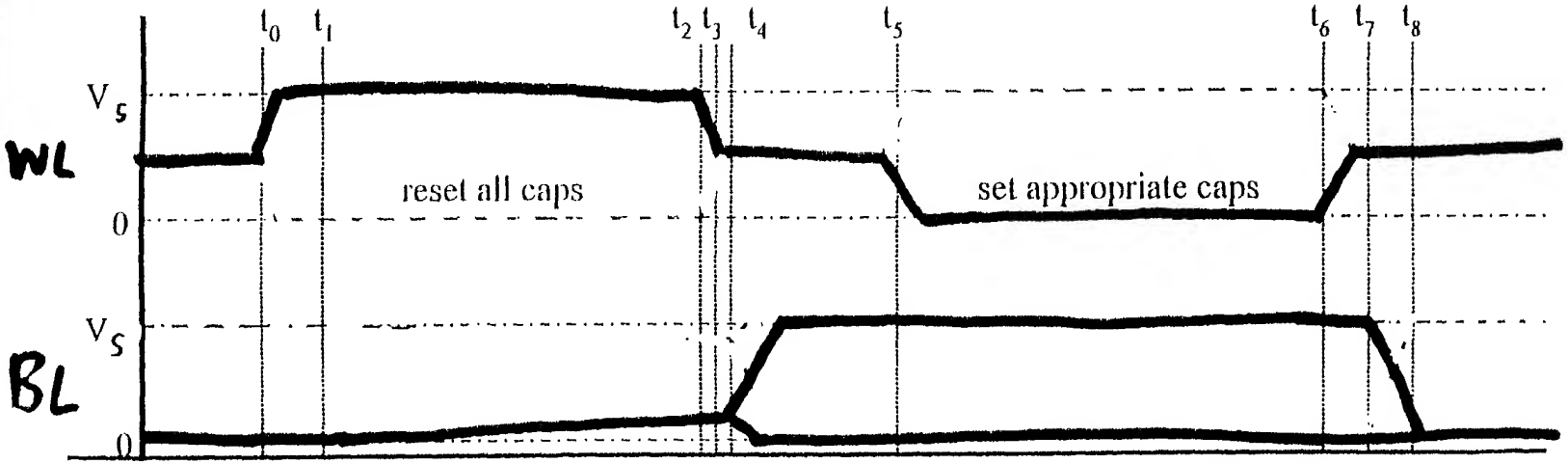
3 *Level Passive Matrix Switching Protocol*

- t_0: word line latched, active pull up to V_s
- t_1: bit line clamp released - sense amp on
- t_2: bit line decision - data latched
- t_3: word line returned to quiescent $V_s/2$
- t_4: write data latched on bit lines
- t_5: word line pulled to 0 - set/reset caps
- t_6: word line returned to quiescent $V_s/2$
- t_7: bit lines actively returned to 0 clamp
- t_8: read/write cycle complete

Maximum depolarizing voltage Vs/2



Sense Amps biased near V_s



Read Cycle

Refresh/Write Cycle

FIG. 5

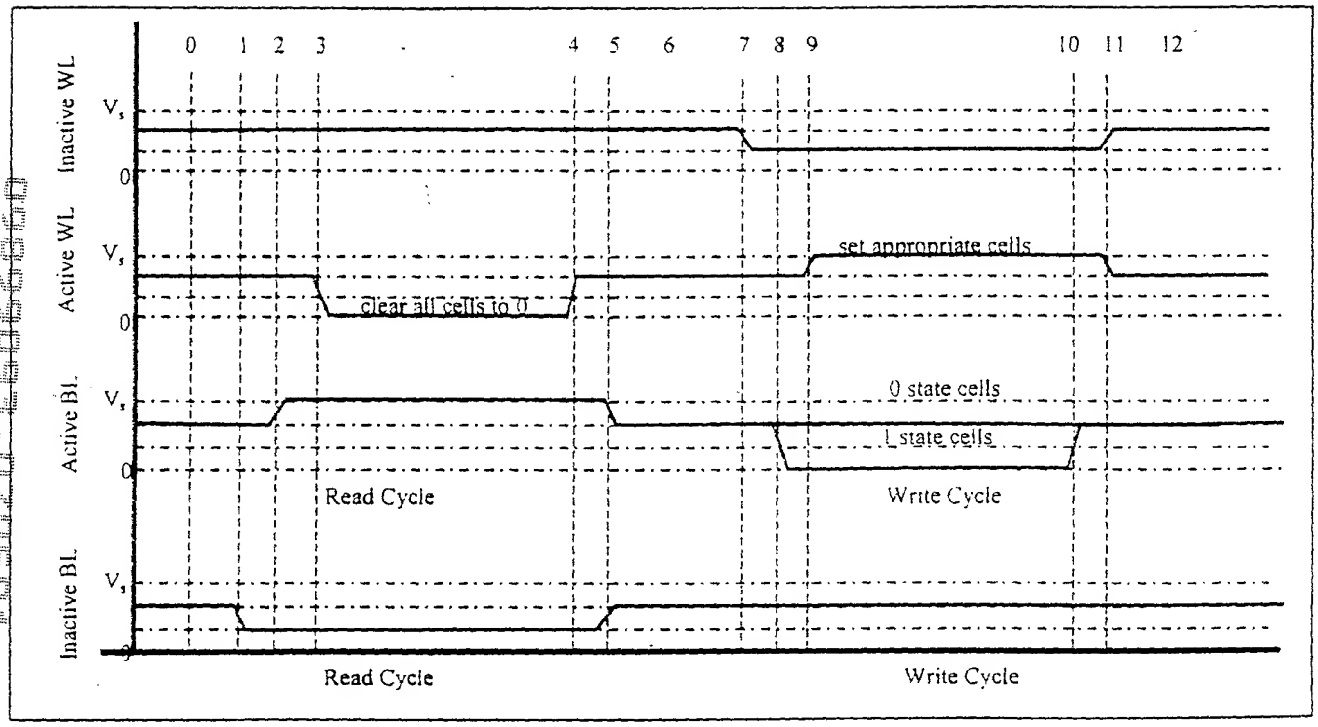

0
1
2
3
4
5
6
7
8
9
10
11
12
Inactive WL
Active WL
Active BL
Inactive BL
V,
0
set appropriate cells
clear all cells to 0
0 state cells
1 state cells
Read Cycle
Write Cycle
Read Cycle
Write Cycle

FIG. 6.

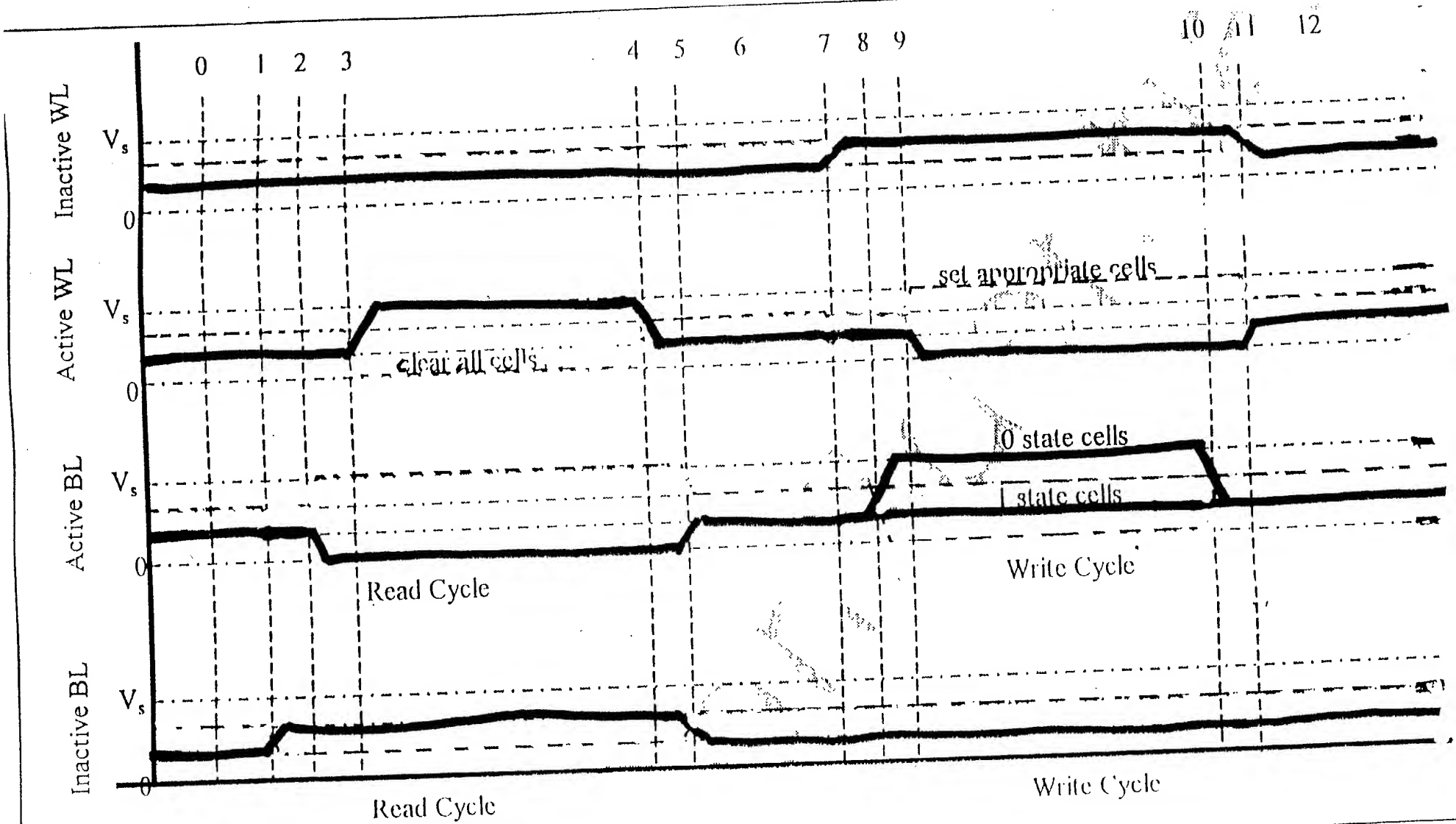


FIG. 7

Five Level Timing Diagram

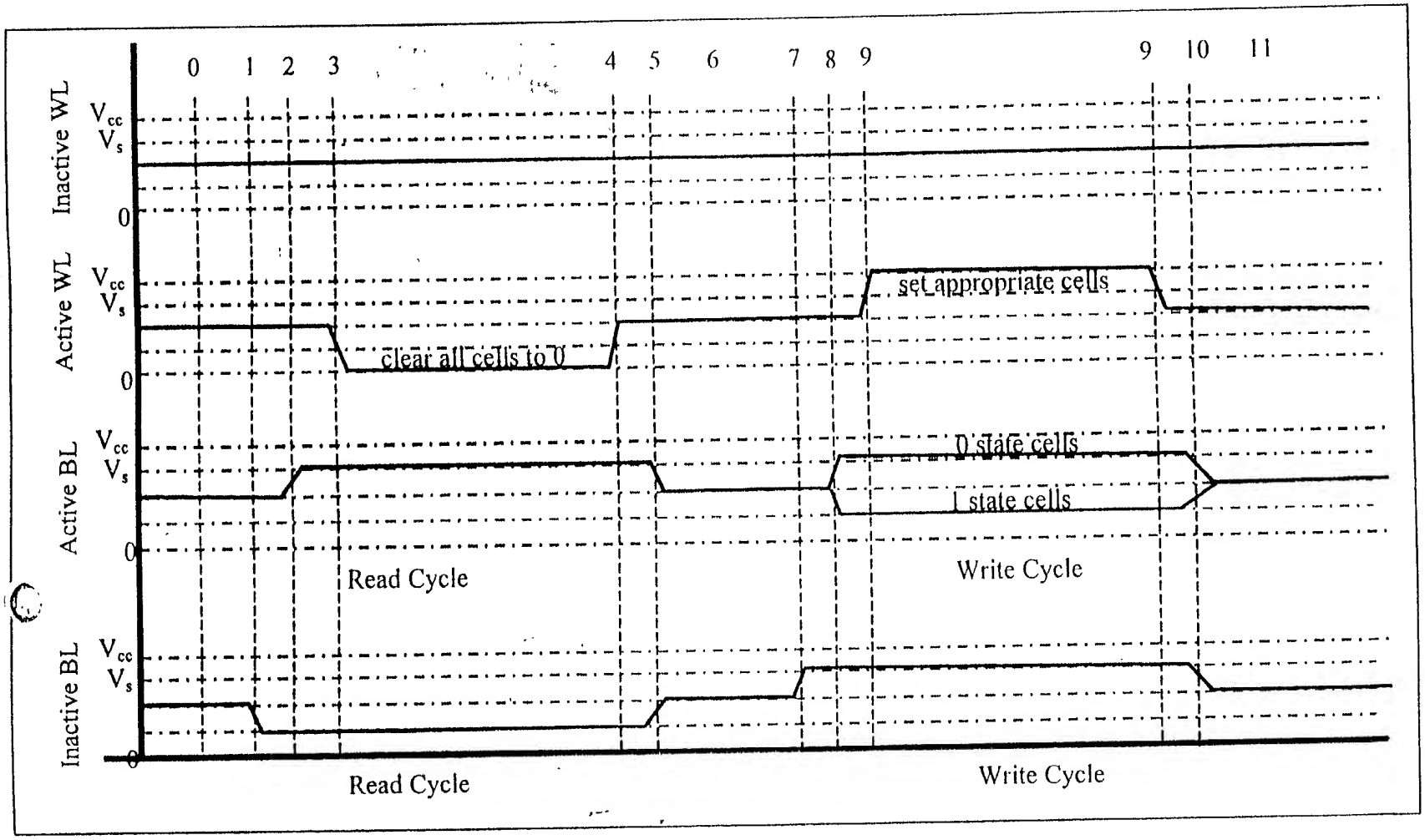


FIG. 8

Five Level Timing Diagram

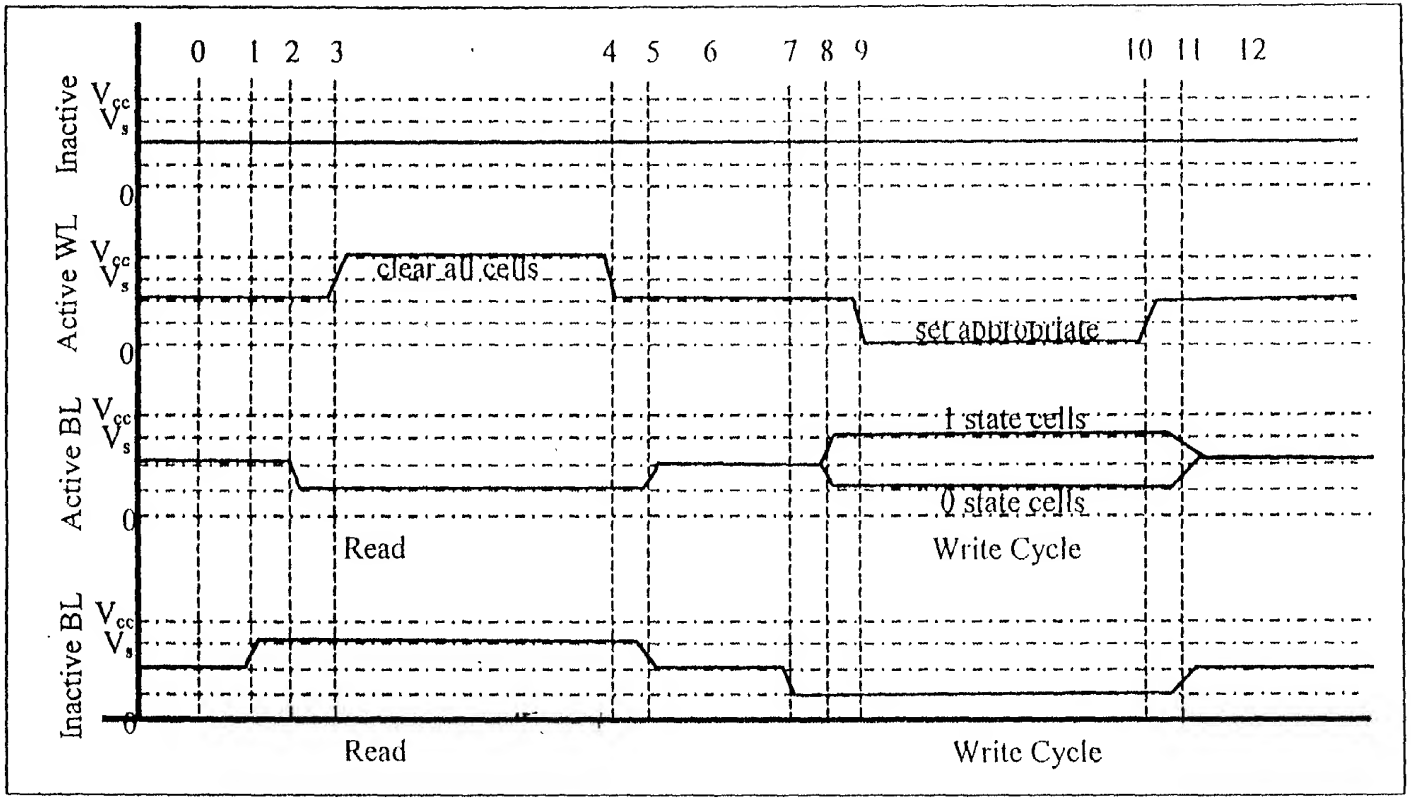


FIG. 9

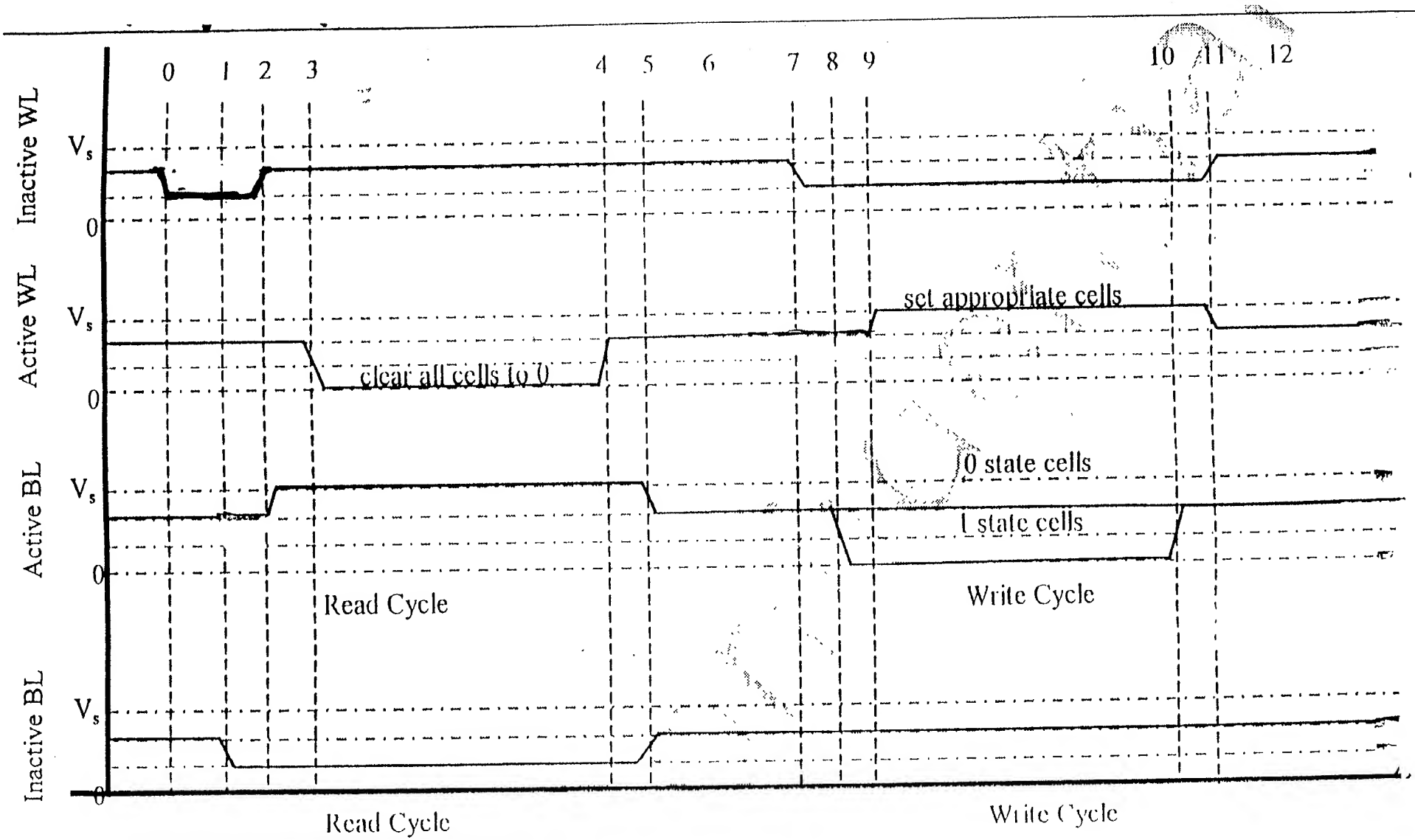

0
1
2
3
4
5
6
7
8
9
10
11
12
Inactive WL
Active WL
Active BL
Inactive BL
V_s
0
clear all cells to 0
set appropriate cells
0 state cells
1 state cells
Read Cycle
Write Cycle
Read Cycle
Write Cycle

FIG. 10

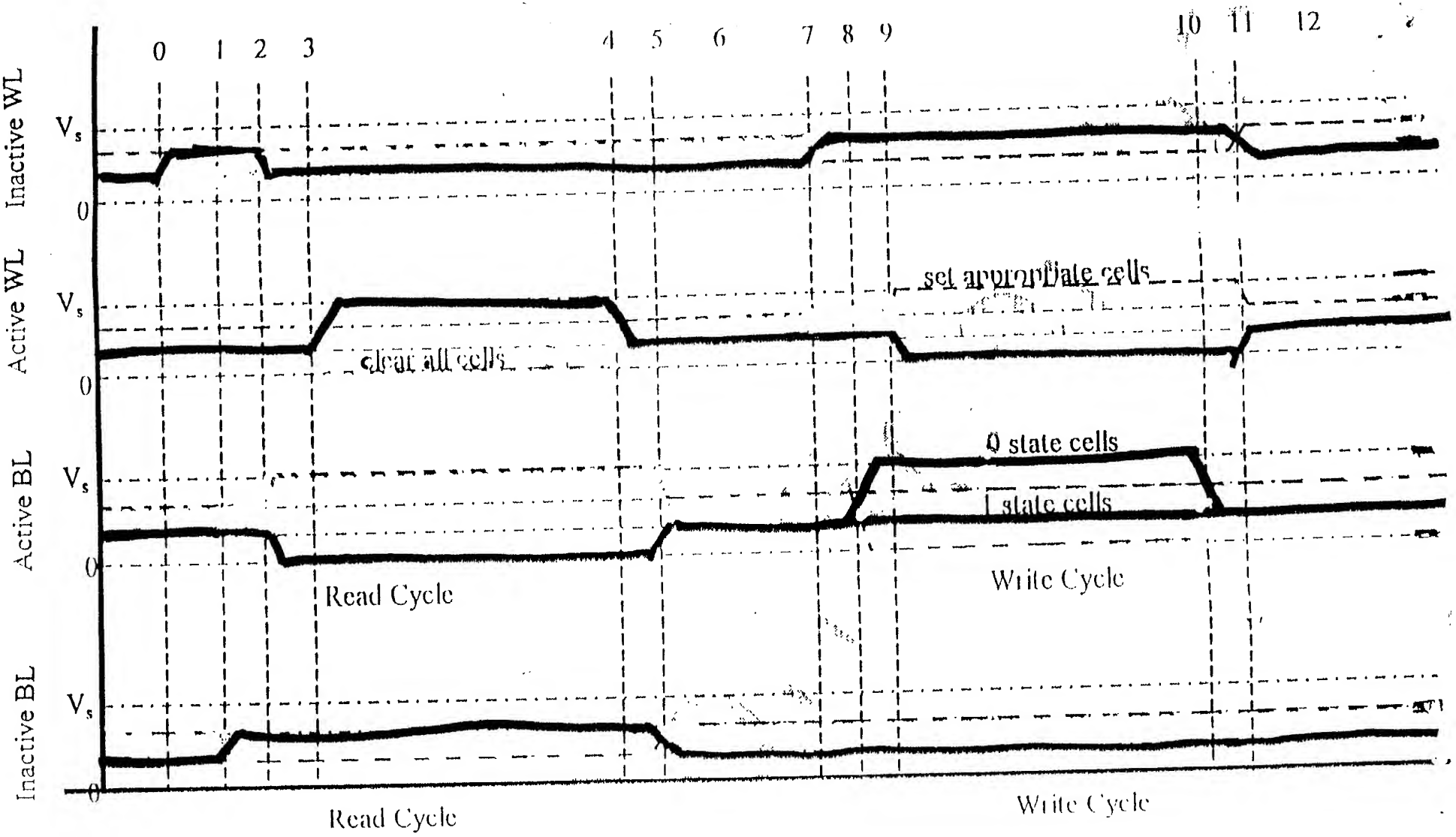


FIG. 11

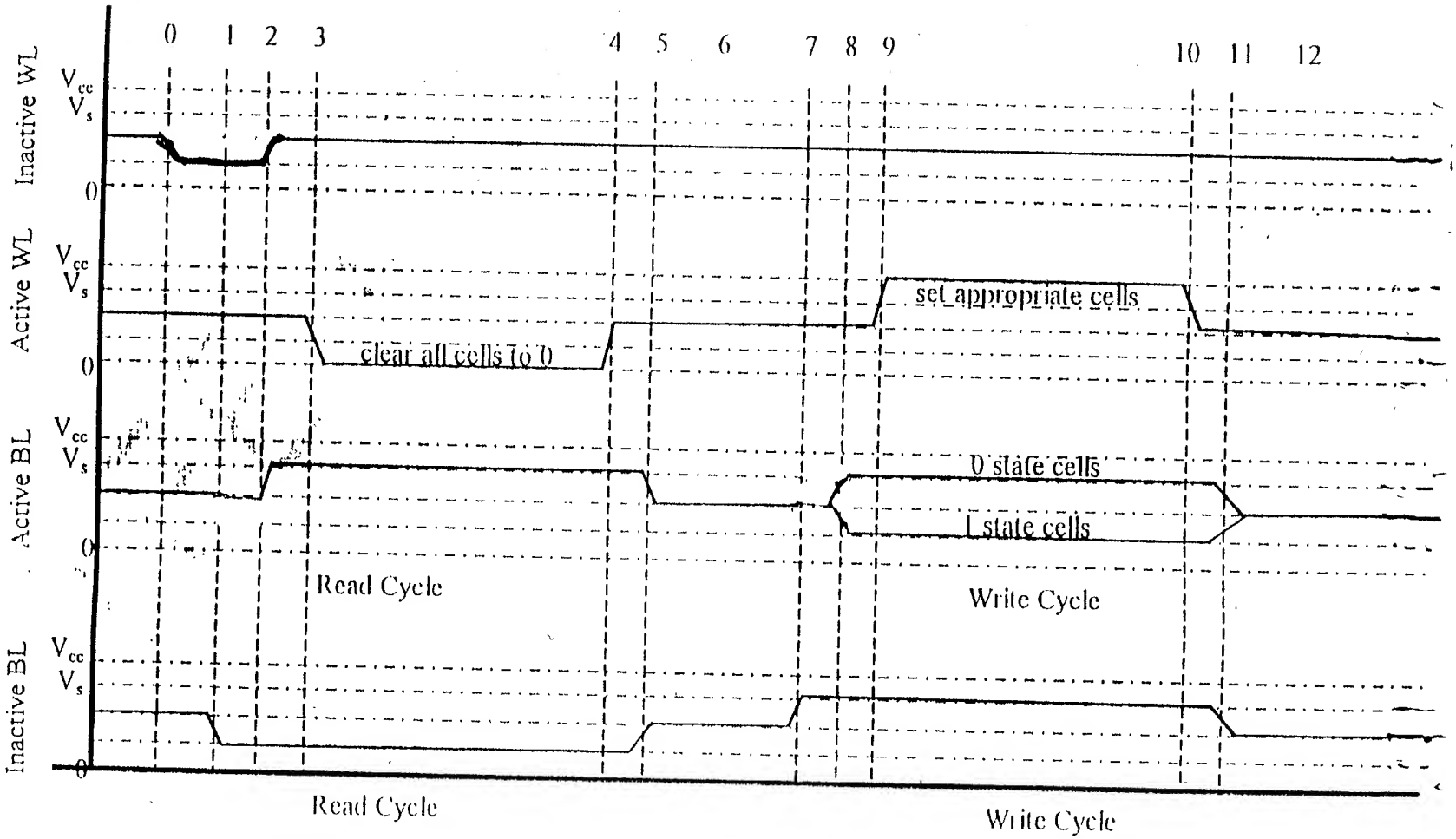

0
1
2
3
4
5
6
7
8
9
10
11
12
Inactive WL
Active WL
Active BL
Inactive BL
V_{cc}
V_s
0
clear all cells to 0
set appropriate cells
0 state cells
1 state cells
Read Cycle
Write Cycle
Read Cycle
Write Cycle

FIG.12

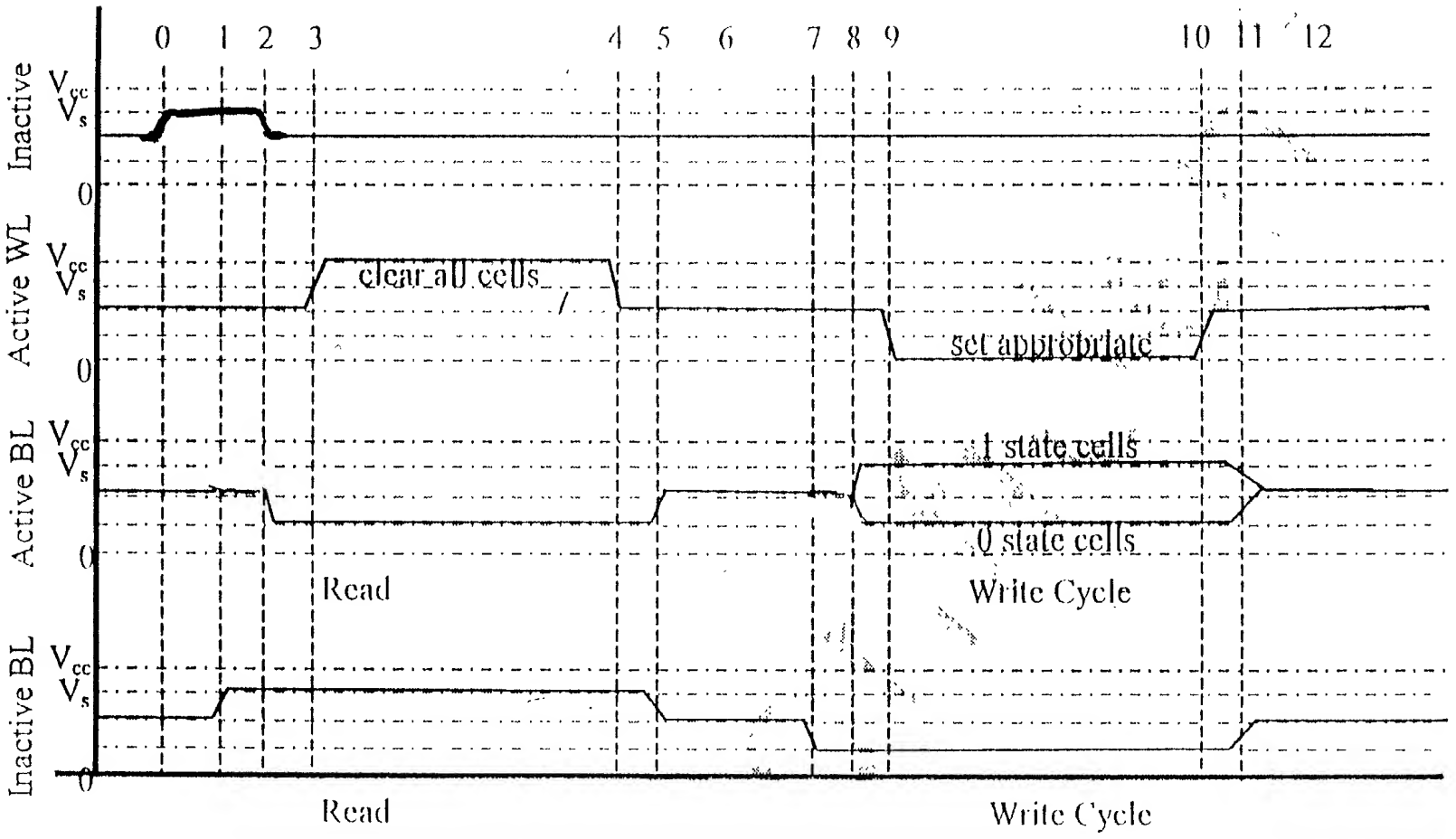

0 1 2 3 4 5 6 7 8 9 10 11 12
Inactive
Active WL
Active BL
Inactive BL
V_{cc}
V_s
0
clear all cells
set appropriate
1 state cells
0 state cells
Read
Write Cycle
Read
Write Cycle

FIG. 13

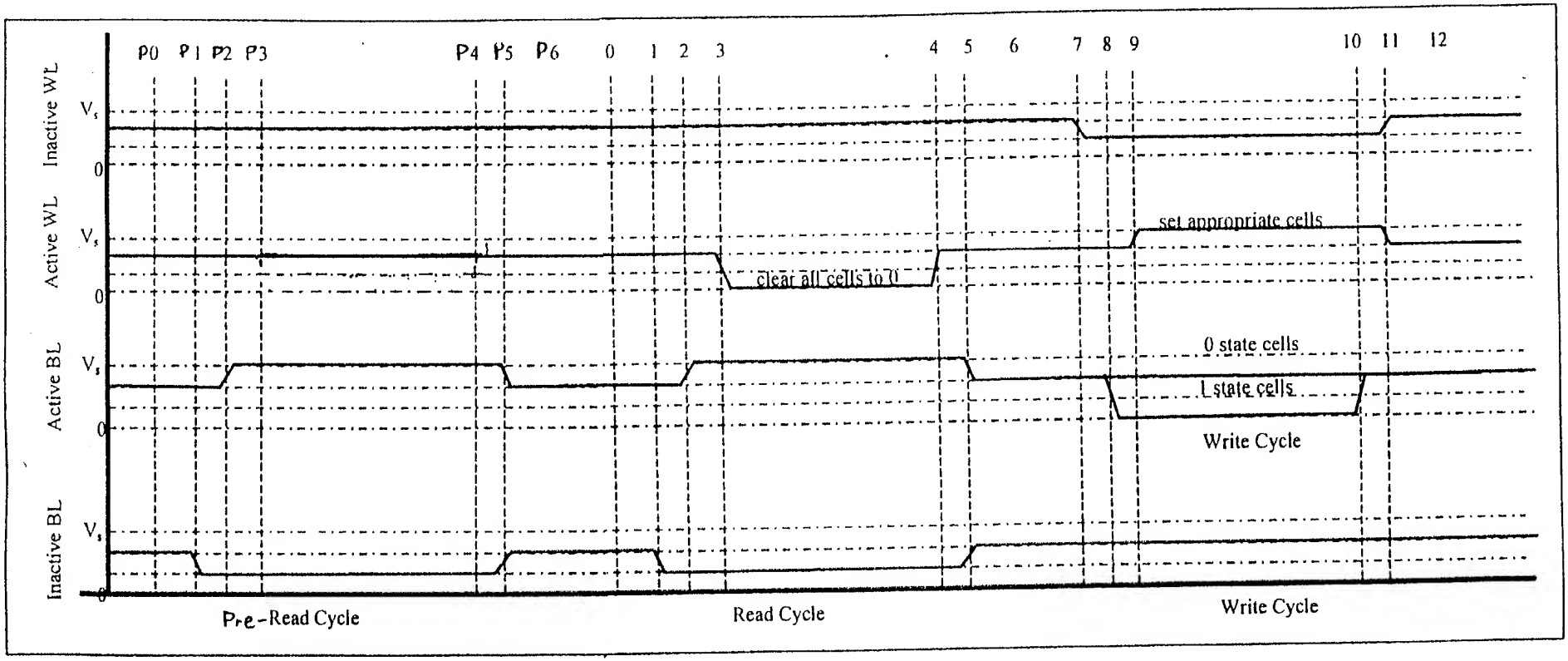


FIG. 14

EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ REFERENCE CYCLE.

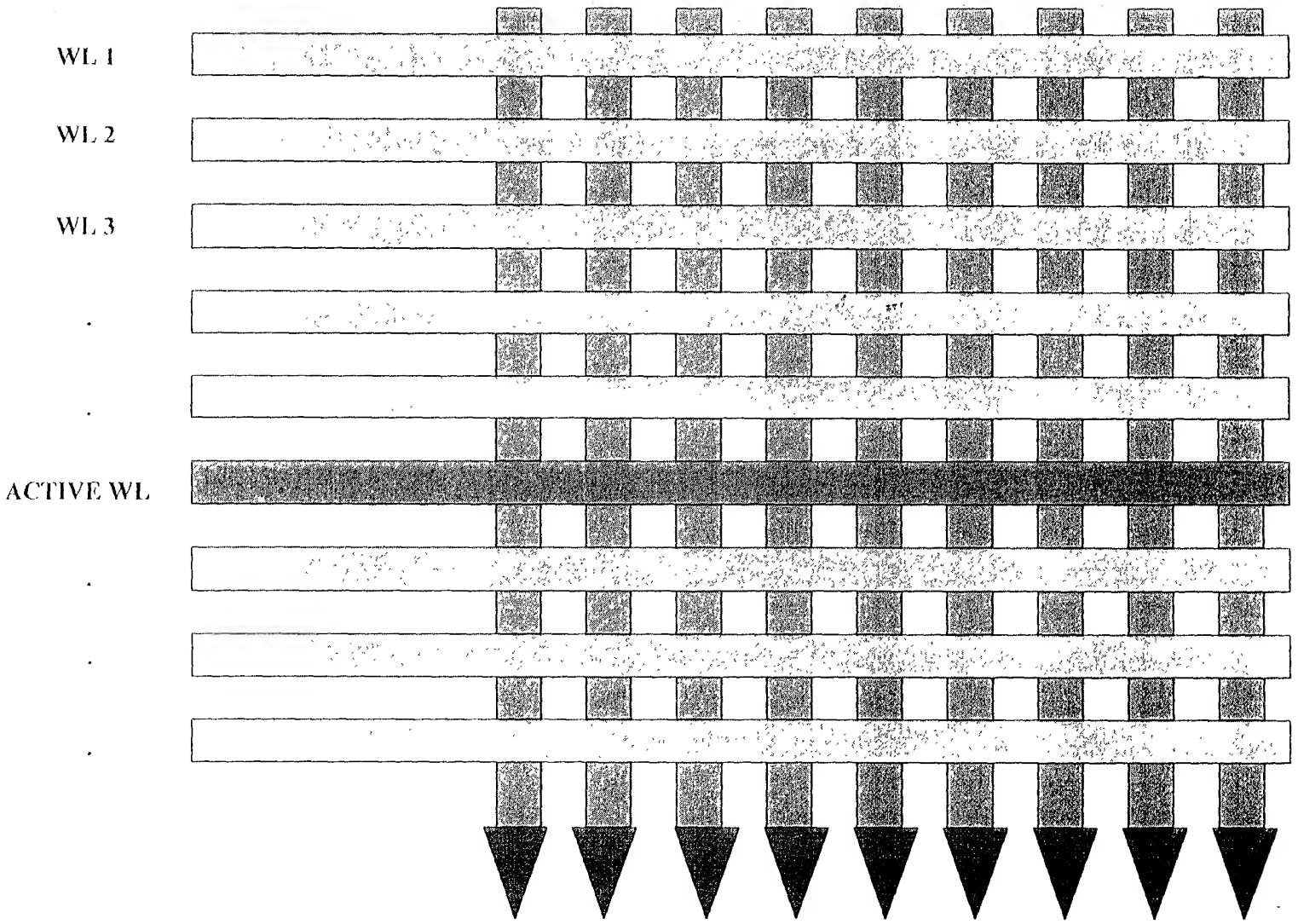


FIG.15